CLAIMS

1. A waveform generator for providing an arbitrary waveform comprising:

a free-running ring oscillator comprising:

a plurality of delay elements connected in a loop; and

a plurality of taps disposed between the delay elements, each tap providing a uniquely phased, oscillating transition signal;

an algebra module having an algebra data input port, a clock input port and an algebra data output port, the algebra module generating a signal at the algebra data output port indicative of a first rising edge of the arbitrary waveform in response to a signal received at the algebra data input port;

a switching module having a switch input port in electrical communication with the algebra data output port, a plurality of switch tap input ports in electrical communication with said plurality of free-running ring oscillator taps and a switch output port, the switch module providing at the switch output port a first transition signal selected from one of the plurality of taps in response to the signal indicative of a first rising edge received at the switch input port; and

an output module having a transition signal input port in electrical communication with the switch output port, a window input port in electrical communication with the algebra data output port and a waveform output port, the output module generating an arbitrary waveform at the waveform output port in response to the first transition signal received at the transition signal

input port of the output module and the signal indicative of a first rising edge received at the window input port.

2. The arbitrary waveform generator of claim 1 further comprising a loop averaging module having a reference clock input port and a tap input port electrically connected to the plurality of taps, the loop averaging module, in response to a reference clock signal received at the reference clock input port, configured to (i) count the number of tap transitions occurring between edges of the reference clock signal and (ii) calculate an average loop speed in response to the count.

3. The loop averaging module of claim 2 further configured to calculate an instantaneous phase of the ring oscillator in response to (i) the calculated average loop speed and (ii) a plurality of captured states of the loop.

4. The arbitrary waveform generator of claim 1 further comprising:

a fine delay module, having a signal input port in electrical communication with the switch output port, a selection input port in electrical communication with the algebra data output port of the algebra module and a fine-delay output port in electrical communication with the input port of the output module, the fine delay module delaying the propagation of the first transition signal from the switch output port of the switching module to the input port of the output module in response to the signal indicative of a first rising edge received at the selection input port;

wherein the input port of the output module is in electrical communication with the switch output port of the switching module through the fine delay module.

5. The arbitrary waveform generator of claim 1 wherein the algebra module further comprises a synchronization input port, the algebra module generating at the algebra data output

port a signal indicative of a first rising edge within the arbitrary waveform in response to a signal received at the algebra data input port and a signal received at the synchronization input port.

6. The arbitrary waveform generator of claim 5 wherein the algebra module generates a signal indicative of a first rising edge that results in a seamless incorporation of the first rising edge in the arbitrary waveform.

7. The arbitrary waveform generator of claim 1 wherein one of the delay elements is an inverting delay element.

8. The arbitrary waveform generator of claim 1 wherein each of the delay elements is identically loaded.

9. The arbitrary waveform generator of claim 1 wherein at least one delay element further comprises a test switch module having a test control input port and a test data input port, the delay element generating at the corresponding tap a signal identical to the signal received at the test data input port in response to a signal received at the test control input port.

10. The arbitrary waveform generator of claim 1 further comprising a compensation module having a data output port in electrical communication with the algebra module and a compensation input port to receive a signal indicative of a frequency altering parameter of a source of a reference clock, the compensation module estimating a variation in a frequency of the reference clock associated with the frequency altering parameter, the compensation module generating a correction signal at the compensation output port in response thereto.

11. The arbitrary waveform generator of claim 10 wherein the frequency altering parameter is a temperature of the source of the reference clock.

12. The arbitrary waveform generator of claim 10 wherein the frequency altering parameter is an age of the source of the reference clock.

13. The arbitrary waveform generator of claim 1 wherein the algebra module is further configured to generate a second signal indicative of a first falling edge within the arbitrary waveform at the algebra data output port in response to a signal received at the algebra input port.

14. The arbitrary waveform generator of claim 1 wherein the output module is further configured to generate a catch-up signal indicative of an erroneous signal indicative of a first rising edge received at the window input port.

15. The arbitrary waveform generator of claim 1 implemented within a CMOS integrated circuit.

16. The arbitrary waveform generator of claim 1 further comprising:

an amplifier feeding forward at least one component of power-supply noise from a power supply coupled to the ring oscillator; and

a loop-speed compensator circuit in electrical communication with said amplifier.

17. The arbitrary waveform generator of claim 1 further comprising:

a plurality of capacitive elements each in electrical communication with a respective one of a plurality of signal paths, each capacitive element having a respective predetermined capacitance to generate a respective predetermined time delay in the propagation of a transition signal through the respective signal path such that the propagation time for a transition on a first signal path is substantially equal to the propagation time for a transition on a second signal path.

18. The arbitrary waveform generator of claim 17 wherein each capacitive element of the plurality of capacitive elements has a value less than approximately 50 femtofarads.

19. The arbitrary waveform generator of claim 17 wherein each one of a plurality of signal paths is in electrical communication with a first capacitive element and a second capacitive element.

20. The arbitrary waveform generator of claim 19 wherein the first capacitive element and the second capacitive element have different sensitivities to temperature.

21. The arbitrary waveform generator of claim 19 wherein the first capacitive element and the second capacitive element have different sensitivities to process.

22. The arbitrary waveform generator of claim 19 wherein the first capacitive element and the second capacitive element have different sensitivities to supply voltage.